REMARKS

Claims 1-4, 7-10, 13-17 and 20-21 are currently pending.

Claims 5-6, 11-12 and 18-19 have been cancelled.

Claims 22-42 have been previously withdrawn.

Reconsideration of Claims 1-4, 7-10, 13-17 and 20-21 is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1-3, 7-9, 13-17 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,902,640 to *Sachitano et al.*, hereinafter "Sachitano". These rejections are respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

The limitations in Claim 1 are not taught or suggested in Sachitano. In particular, Sachitano does not teach or suggest that a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants, as required by independent Claim 1.

The January 10, 2007 Office Action stated that "Regarding Claim 1, Sachitano et al. discloses a semiconductor apparatus comprising a double-poly bipolar transistor (fig. 12, 114) and a double-poly metal oxide semiconductor (MOS) transistor (120), wherein a base of the double-poly bipolar transistor (140) and a gate of the double-poly MOS transistor (148) contain substantially identical dopants (both NPN and PNP devices are disclosed; col. 1, lines 63-66. PNP devices would inherently have an n-type base, which is substantially identical to the n-type dopant of the MOS gate (148)." (January 10, 2007 Office Action, Page 2, Line 21 to Page 3, Line 2). For the reasons set forth below, the Applicants respectfully traverse these assertions.

The January 10, 2007 Office Action relies on a principle of inherency, stating that "PNP devices would inherently have an n-type base, which is substantially identical to the n-type dopant of the MOS gate 148." The Examiner is correct that a PNP bipolar transistor does have an n-type base by definition, but the Examiner is incorrect in therefore concluding that this has anything to do with the dopant of the MOS gate 148.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' "*In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations

omitted, emphasis added).

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The Examiner has not provided any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art, as he is required, and so the allegation of inherency cannot support the rejection.

An n-type base, as known to those of skill in the art, is simply a transistor base in which the conduction electron density exceeds the hole density. A PNP bipolar transistor does have an n-type base.

A dopant, as known to those of skill in the art, is an impurity that is added to a semiconductor to change the number of holes and electrons relative to each other, and an n-type dopant is an impurity that "donates" weakly-bonded electrons to the semiconductor. There are different n-type dopants – phosphorus and arsenic are both n-type dopants, but are not "substantially identical". Certainly an n-type base is not substantially identical an n-type dopant, as alleged by the Examiner, as these are very different things. Further, to different n-type semiconductor elements do not necessarily have substantially identical dopants, so the claimed limitation is not an inherent feature of Sachitano, as alleged. In fact, Applicant respectfully submits that Sachitano appears to suggest differentiated doping during formation. (Column 4,

Line 55 to Column 5, Line 7; Column 10, Lines 31-51).

For reference purposes, the Applicants set forth below an outline of certain major steps in the manufacture of the Applicants' invention.

A. Paragraph [00112] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the PNP device and an NMOS gate in the NMOS device.

B. Paragraph [00114] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the NPN device and a PMOS gate in the PMOS device.

C. Paragraph [00129] describes how the intrinsic base (3410) in the NPN device is doped and how the lightly doped drains (LDD) (3420, 3430) in the PMOS device are doped.

D. Paragraph [00132] describes how the intrinsic base (3510) in the PNP device is doped and how the lightly doped drains (LDD) (3520, 3530) in the NMOS device are doped.

E. Paragraph [00138] describes how the Poly 2 layer (3800) is doped to form (1) NPN emitter 3910 in the NPN device, and (2) NPN deep collector 3920 in the NPN device, and (3) NMOS source/drain 3930 in the NMOS device, and (4) PMOS well contact 3940 in the PMOS device.

F. Paragraph [00141] describes how the Poly 2 layer (3800) is doped to form (1) PNP emitter 4010 in the PNP device, and (2) PNP deep collector 4020 in the PNP device, and (3) NMOS well contact 4030 in the NMOS device, and (4) PMOS source/drain 4040 in the PMOS device.

Now consider the structure and method disclosed in the Sachitano reference.

Before the first polysilicon layer 134 is deposited in Step 29, there is a first implant step (Step 25) that is carried out for the "gate threshold voltages" of the MOS devices. Then there are two implant steps (Steps 26 and 27) that are performed "to implant collector contact region 130 to an increased N+ concentration" in the NPN device (Sachitano, Column 8, Lines 6-12). It is noted that Step 25, Step 26 and Step 27 are performed sequentially. Then the polysilicon layer 134 is deposited. (Step 29) (Sachitano, Column 8, Lines 17-19).

Sachitano then states "This layer [first polysilicon layer 134] is then masked and implanted, first, to implant the polysilicon layer to N+ concentrations over the PMOS and NMOS active device regions and over the collector contact region 130 (steps 30 and 31)." (Sachitano, Column 8, Lines 19-22). This first implant step includes the "gate" portions of the PMOS and NMOS devices. (See Figure 4 of Sachitano).

Then the N+ implant mask is stripped and the substrate is again masked and the first polysilicon layer 134 is "implanted to dope the polysilicon layer overlying the NPN bipolar active region to P+ concentrations (steps 32 and 33)." (Sachitano, Column 8, Lines 23-26). This second implant step includes the "base" portions of the NPN device. (See Figure 4 of Sachitano).

The PMOS and NMOS active device regions of the Sachitano device are implanted to N+ concentrations using an N type dopant (e.g., arsenic, antimony, phosphorus). Table 1 in Column 12 of Sachitano describes the use of phosphorus as the N type dopant. The bipolar NPN device region of the Sachitano device is implanted to P+ concentrations using a P type dopant (e.g., boron, indium, gallium, aluminum). Table 1 in Column 12 of Sachitano

describes the use of boron as the P type dopant. This clearly shows that the dopants that are used by Sachitano are not substantially identical.

Sachitano later implants the base region 150 of the NPN transistor. "Masking and boron implant steps (steps 37 and 38) provide P-type base region 150 for the bipolar transistor in region 114 and lightly-doped P-source and drain regions 152, 154 for the PMOSFET in region 118." (Sachitano, Column 8, Lines 45-49). Sachitano described a single implant step for the base of the NPN transistor and the lightly doped source/drain regions of the PMOS transistor. However, this implantation does not affect the shielded gate regions of the MOS transistors.

For the reasons set forth above, the Applicants respectfully submit that the Sachitano reference does not teach or suggest that "a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants." The Applicants respectfully submit that this feature is not inherent in the Sachitano reference.

Accordingly, the Applicants respectfully traverse all of the anticipation rejections of Claims 1-3, 7-9, 13-17 and respectfully requests the Examiner to withdraw the § 102 rejections with respect to these claims.

II. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 4, 10 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sachitano in view of U.S. Patent No. 6,441,441 to *Suda*, hereinafter "Suda". The Applicants respectfully traverse these rejections. The Applicants reiterate and incorporate by reference all of the comments and arguments previously made with respect to the Sachitano reference.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

The January 10, 2007 Office Action stated that "Sachitano et al. discloses all of the elements of the claims as discussed in paragraph 3 above, . . . " (January 10, 2007 Office Action, Page 4, Lines 20-21). For the reasons previously set forth, the Applicants respectfully traverse this assertion. The Sachitano reference does not disclose all of the elements of the claims that were discussed in Paragraph 3 of the January 10, 2007 Office Action.

Claims 4, 10 and 20 each require that "at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor," where the base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants. The Examiner is correct that Sachitano does not teach or suggest this feature, as discussed at length above. The Examiner looks to Suda for this teaching. The Applicants respectfully submit that the Suda reference does not remedy the deficiencies of the Sachitano reference.

Suda describes, variously, a PMOS transistor and an NPN bipolar transistor, and indicates in each case that boron is acceptable as a P-type dopant. Suda does not explicitly teach that these two structures contain substantially identical dopants, and certainly one could be heavily doped while the other is lightly doped.

Even if Suda did include such a teaching as alleged by the Examiner, there is no proper motivation to combine these references. The motivation to combine or modify must be specific to the actual teachings sought to be combined. "In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention" *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001) (emphasis added). "When the references are in the same field as that of the applicant's invention, knowledge thereof is presumed. However, the test of whether it would have been obvious to select specific teachings and combine them as did the applicant must still be met by identification of some suggestion, teaching, or motivation in

the prior art, arising from what the prior art would have taught a person of ordinary skill in the field of the invention." (*In re Dance*, 160 F.3d 1339, 1343 (Fed. Cir. 1998) (emphasis added).

The Examiner's alleged motivation is not found anywhere in the art of reference, and nothing in Sachitano or Suda indicate that they are at all concerned with operations as a surface channel device or any particular degradation effects. Nothing in the art of reference, nor in the knowledge generally available to those of skill in the art at the time of the invention, would motivate one to make the specific combination and modification necessary to produce the claimed invention.

The Applicants respectfully submit that one of ordinary skill, having only Sachitano before him, would not be prospectively moved to spontaneously assume that the substantial disclosure of Sachitano was in need of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants. In fact, the Applicants respectfully submit that Sachitano appears to suggest differentiated doping during formation. (Column 4, Line 55 to Column, Line 7; Column 10, Lines 31-51).

In order to overcome the admitted deficiencies of Sachitano, the Examiner selectively culls from Suda the **inference** of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though Suda itself does not explicitly teach that these two structures contain substantially identical dopants. The Examiner further ignores the fact that, in order to combine the references as suggested, one of ordinary skill in the art would have to completely overlook the remainder of Suda's various teachings of PMOS transistor and an NPN bipolar transistor structure and

formation – teachings that vary significantly from Sachitano's.

The Examiner offers that "P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor" (January 10, 2007 Office Action, Page 5, Lines 7-8) as the motivation for one of ordinary skill in the art to embark on this speculative and selective combination process. This has no bearing at all on the Applicants' use of substantially identical dopants, as claimed.

In summary, there is neither a motivation nor a suggestion in either the cited references or the knowledge of a person of ordinary skill in the art at the time of the Applicant's invention to: 1) spontaneously assume a deficiency in Sachitano; 2) seek out and find Suda; 3) ignore almost all of Suda's teachings of structure and process; 4) selectively cull a single concept from Suda – a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though Suda does not explicitly disclose such; and 5) substantially modify the processes and structures of Sachitano to incorporate this spontaneous extraction of concept from Suda. Furthermore, even if the references were to be so selectively combined, the combination would still not result in the Applicant's invention as recited in independent Claim 1 or dependent Claims 4, 10 and 20 of the patent application.

Accordingly, the Applicants respectfully request the Examiner to withdraw the § 103 rejections with respect to Claims 4, 10 and 20.

All claim rejections are respectfully traversed. Reconsideration and allowance of the pending claims (Claims 1-4, 7-10, 13-17 and 20-21) are respectfully requested.

III. ADDITIONAL COMMENTS

In the Sachitano reference, both the PMOS device and NMOS device are doped with an N type dopant (phosphorus). The Sachitano reference also uses a separate mask and a P type implant (boron) for the NPN extrinsic base. While in the case of providing only an NPN device, this mask count is mask count neutral when compared to the mask count of the Applicants' invention. This is because the Sachitano reference uses a single mask for the PMOS and NMOS active regions. However, in making complementary BiCMOS the Sachitano method would require an additional mask for the PNP extrinsic base. In contrast, in making complementary BiCMOS the Applicants' invention would save one mask and implant procedure.

The Sachitano method also adds a separate intrinsic base implant. This is because it includes the PMOS PLDD in the NPN intrinsic base but adds an additional dedicated mask and implant to augment the base doping. In contrast, the Applicants' invention uses the same mask and implant to form the PLDD and the NPN intrinsic base and the NLDD and the PNP intrinsic base. In the case of complementary bipolar or complementary BiCMOS, this feature saves two masking layers and implants (and the associated cycle time and costs) over the prior art.

The complementary doping of the MOS gates in the Applicants' invention enables complementary doping of the extrinsic base and, therefore, the formation of both NPN devices and PNP devices. The complementary doping of the gates provides better threshold matching and control. For these reasons, the Applicants' invention provides significant improvements over the technology that is disclosed in the prior art.

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SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

No fees are believed to be necessary. However, in the event that any fees are required for the prosecution of this application (including extension of time fees), the Commissioner is hereby authorized to charge any necessary fees to Deposit Account No. 50-0208.

Respectfully submitted,

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